

Figure 1

200

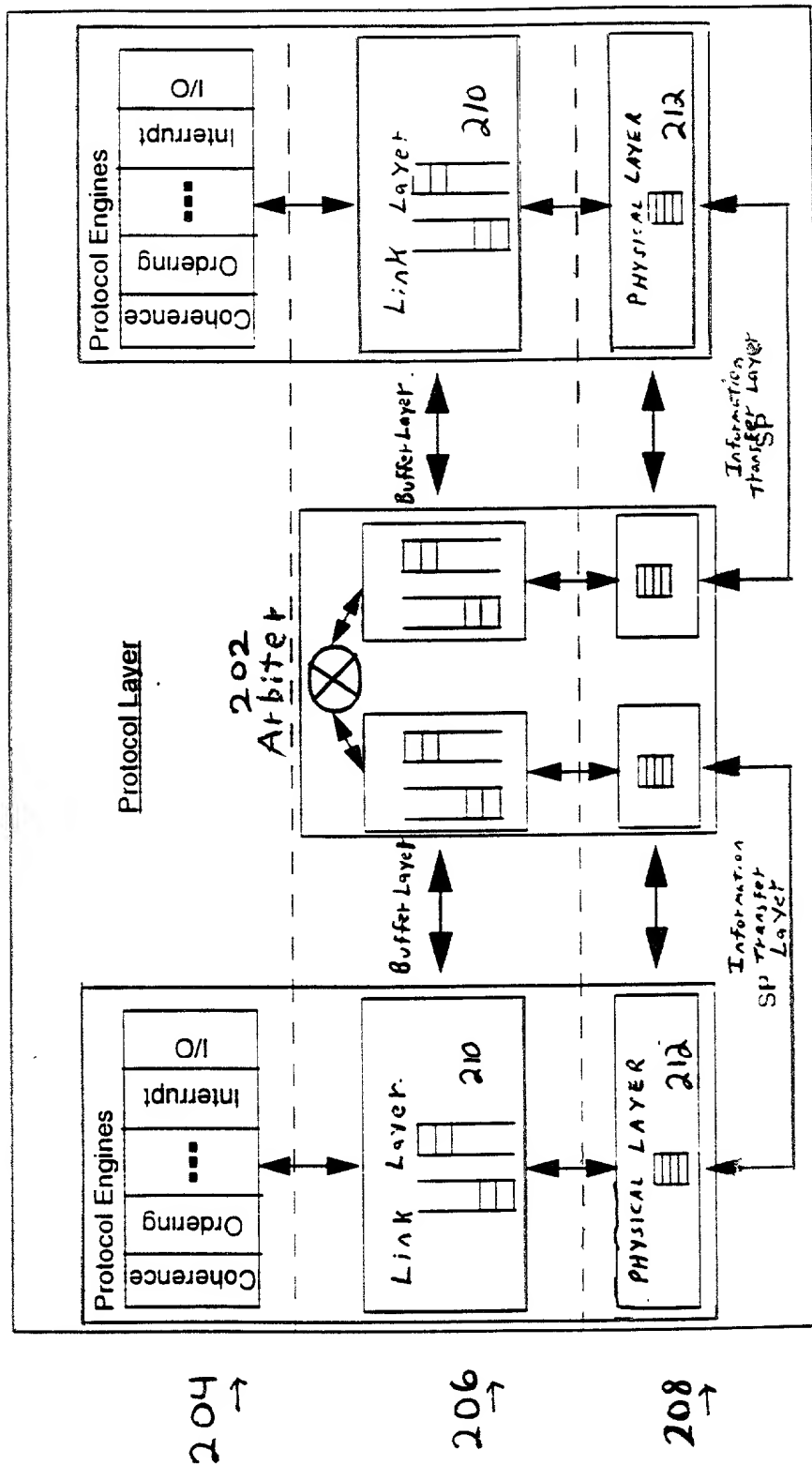


Figure 2

FIG. 3 is a block diagram of a system 300 according to one embodiment of the present invention. The system 300 includes a first processor 304 and a second processor 306. The first processor 304 and the second processor 306 are connected to an input-output component 314. The first processor 304 is connected to the input-output component 314 via a 16-bit bus 310. The second processor 306 is connected to the input-output component 314 via a 16-bit bus 312. The first processor 304 and the second processor 306 are also connected to each other via a 48-bit bus 308.

300

48 bit

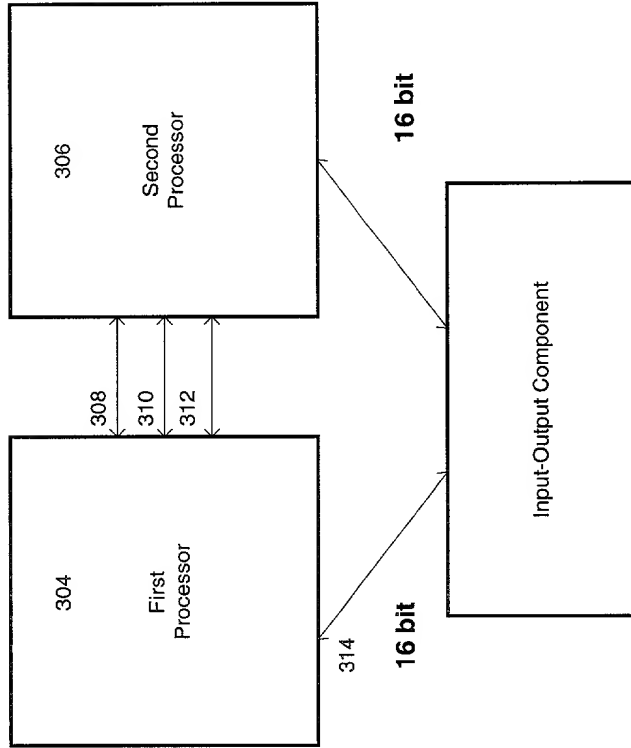


Figure 3

400

32 bit

404

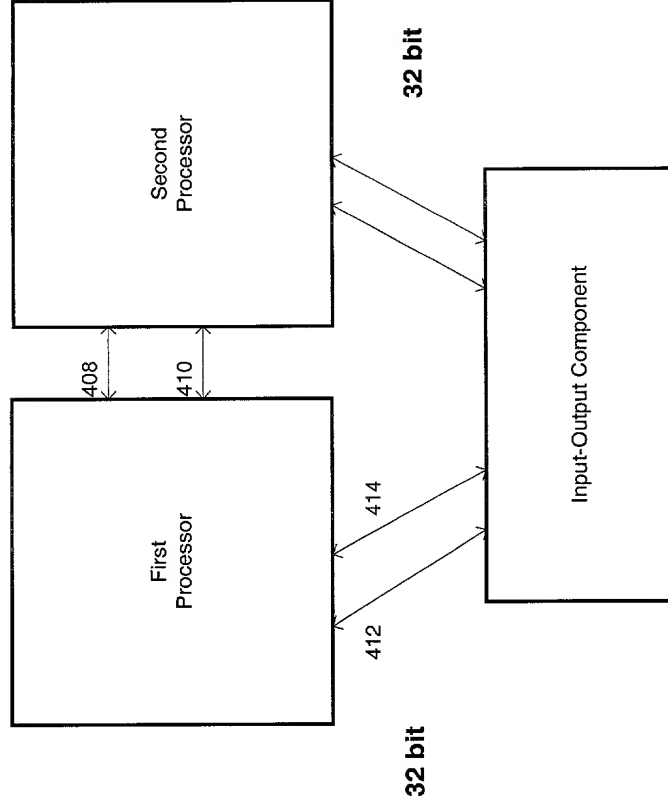


Figure 4

500

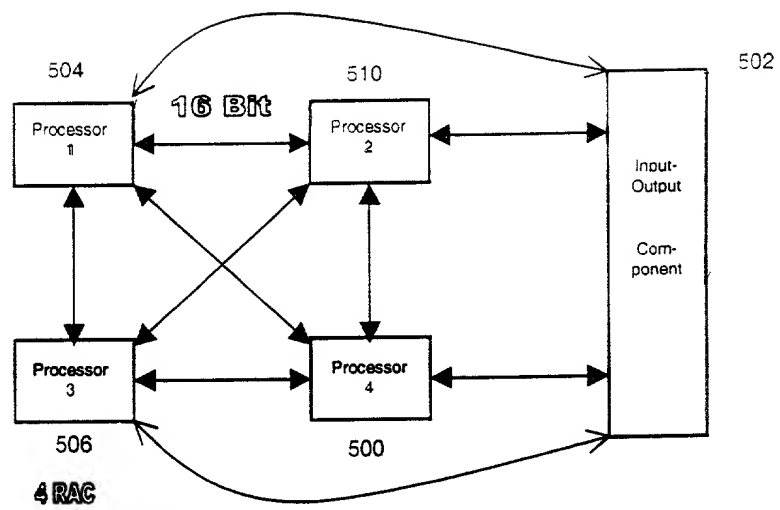


Figure 5

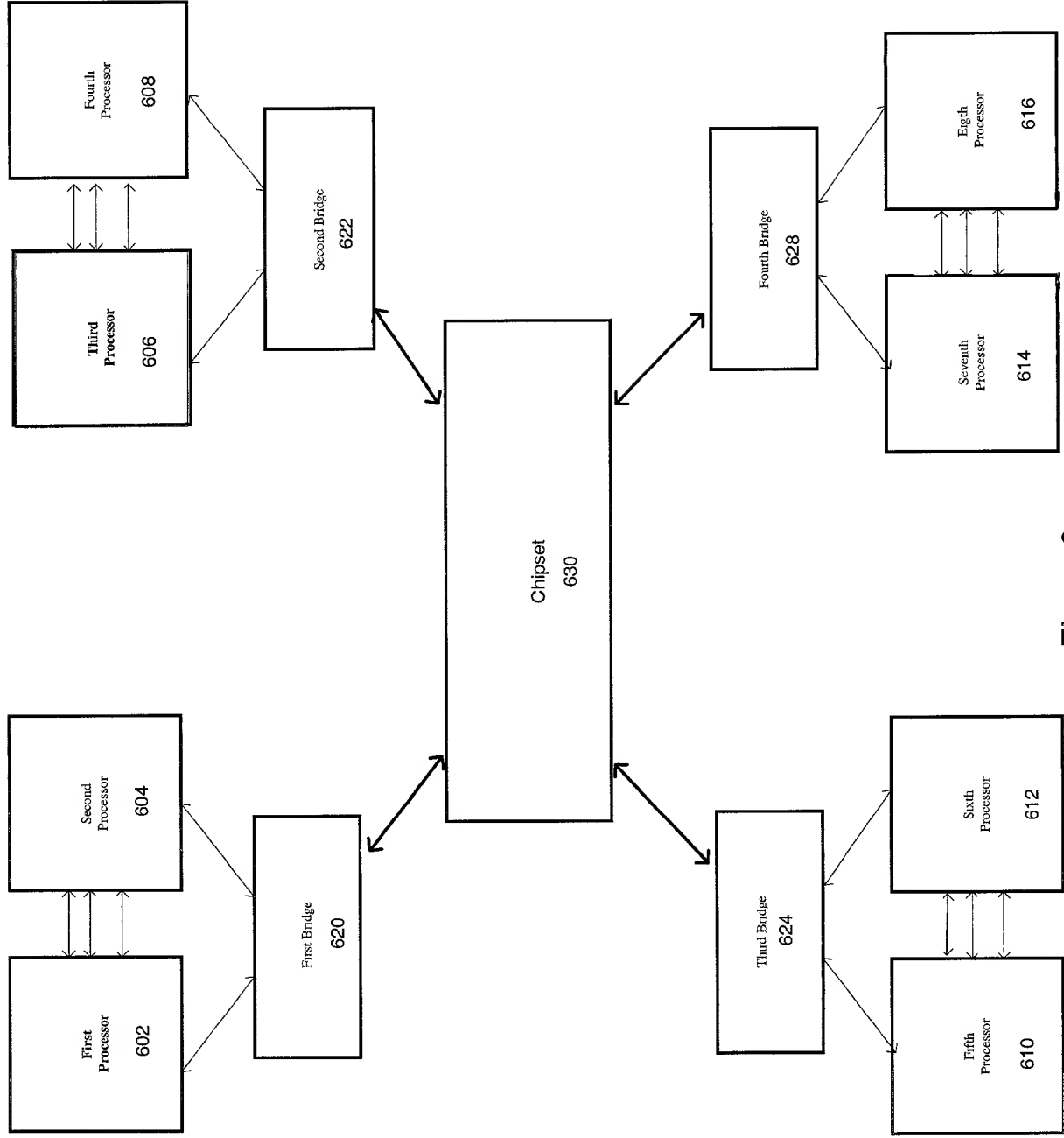


Figure 6

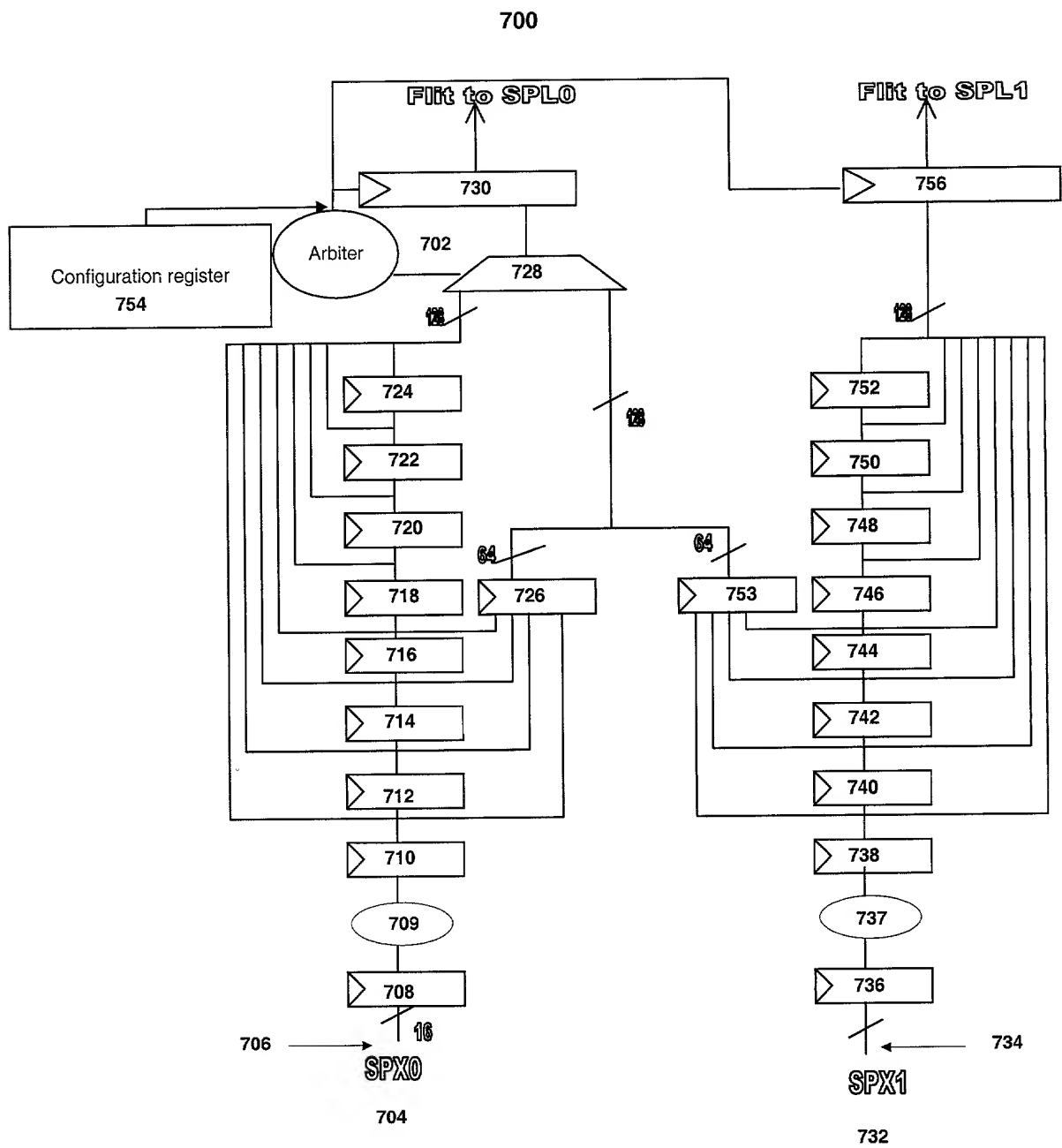


Figure 7

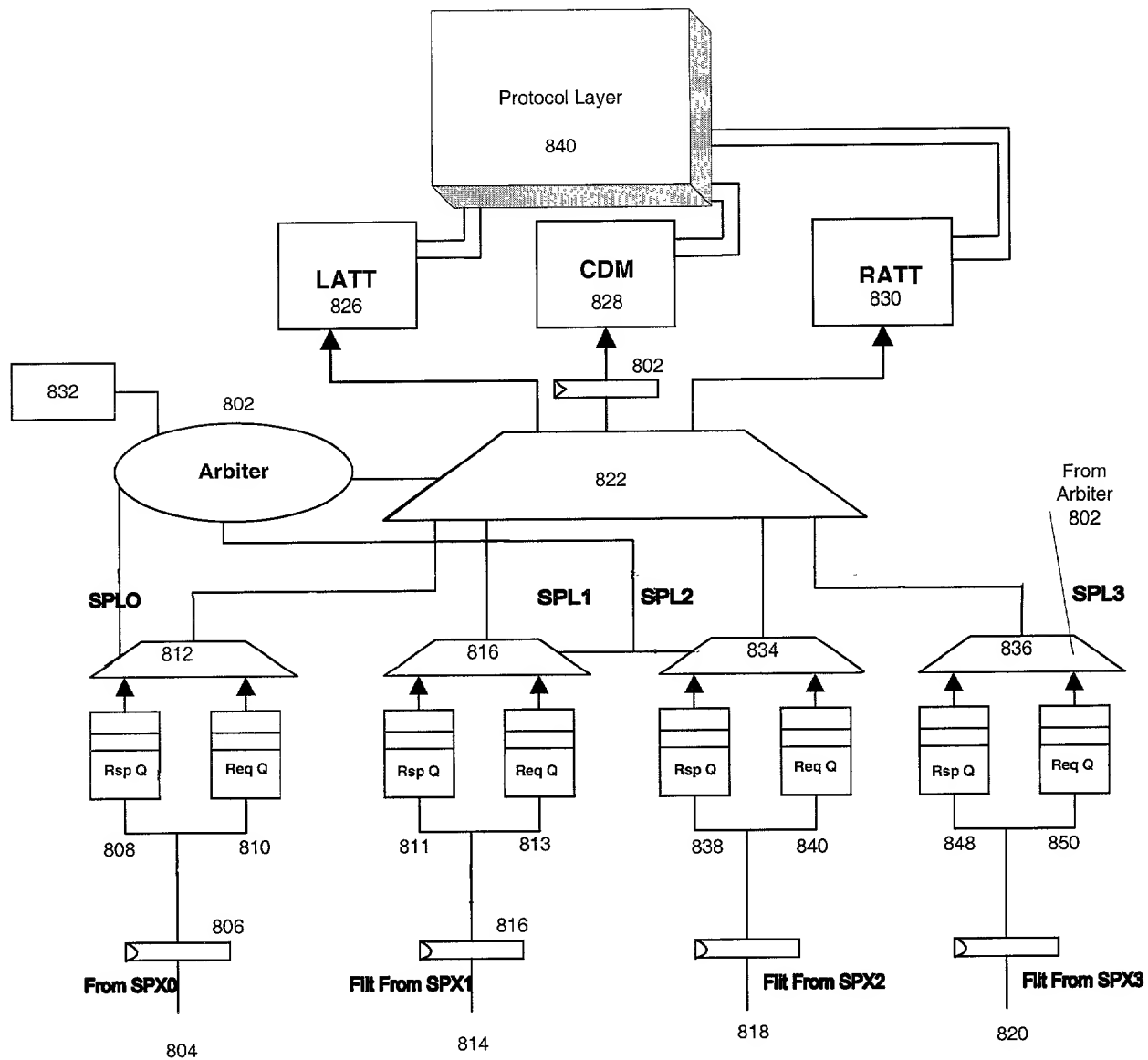


Figure 8

800

900
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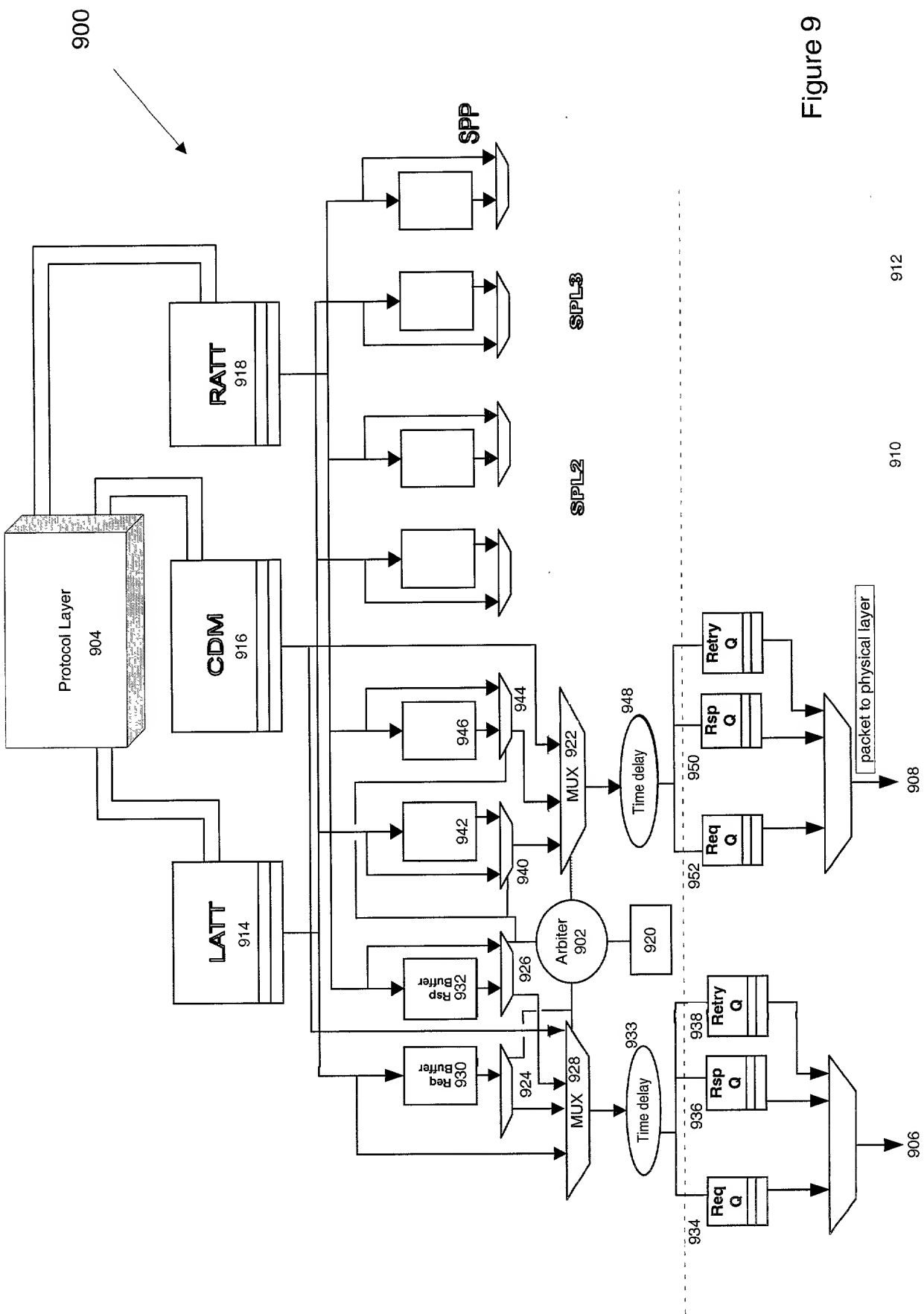


Figure 9

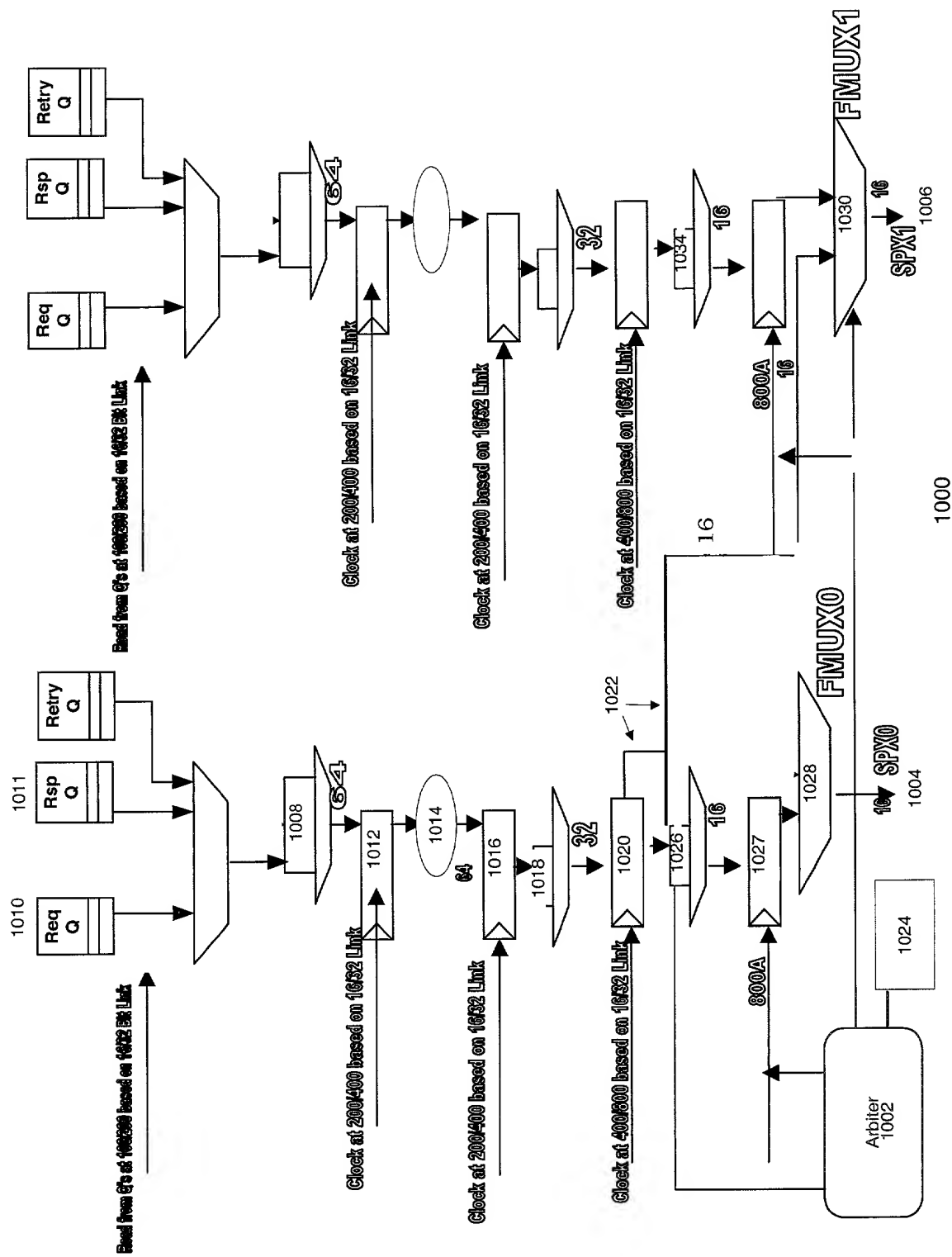


Figure 10